

**AMENDMENTS TO THE CLAIMS:**

**Please amend the claims as follows:**

1. (Currently Amended) An apparatus for estimating power consumption, comprising:  
    ~~an~~ a behavioral synthesis unit to which an algorithm-level description is input for converting the algorithm-level description to a clock-based description and behavioral synthesis information; and  
    a clock-based simulation unit to which the clock-based description and behavioral synthesis information are input for executing a clock-based simulation and calculating a power consumption factor of a storage element based upon both the clock-based description and behavioral synthesis information.
2. (Currently Amended) The apparatus according to claim 1, wherein the power consumption factor of the storage element is calculated by discriminating ~~the~~ a type of the storage element using the behavioral synthesis information in regard to an array-variable part.
3. (Currently Amended) The apparatus according to claim 1, wherein the power consumption factor ~~is~~ comprises toggle rate and/or transition probability.
4. (Currently amended) The apparatus according to claim 2, wherein the power consumption factor ~~is~~ comprises toggle rate and/or transition probability.
5. (Currently amended) The apparatus according to claim 1, wherein a correspondence between RT variable names and gates is assumed from the behavioral synthesis information, and toggle rates and/or transition probabilities are set in gate circuits, thereafter the toggle rates and/or transition probabilities of all gate circuits being calculated.
6. (Original) The apparatus according to claim 3, wherein if a gated clock is provided, the toggle rate and/or transition probability of a clock are made the same as the write probability with respect to a storage element.

7. (Currently Amended) A method of estimating power consumption, comprising the steps of:

inputting a clock-based description and behavioral synthesis information;  
executing a clock-based simulation based upon the clock-based description; and  
calculating a power consumption factor based upon both the clock-based description and behavioral synthesis information.

8. (Currently amended) The method according to claim 7, further comprising a step of:  
calculating the power consumption factor of the storage element by discriminating the  
a type of the storage element, using the behavioral synthesis information, in regard to an  
array-variable part.

9. (Currently Amended) The method according to claim 7, wherein the power consumption factor is comprises toggle rate and/or transition probability.

10. (Currently Amended) The method according to claim 8, wherein the power consumption factor is comprises toggle rate and/or transition probability.

11. (Currently amended) The method according to claim 9, further comprising the steps of:  
assuming a correspondence between RT variable names and gates from the behavioral synthesis information; and,  
setting toggle rates and/or transition probabilities in gate cireuits, circuits; and,  
thereafter, calculating the toggle rates and transition probabilities of all gate circuits.

12. (Original) The method according to claim 9, wherein if a gated clock is provided, the toggle rate and/or transition probability of a clock are made the same as the write probability with respect to a storage element.

13. (New) A method of simulation of a device, said method comprising:  
providing, into a clock-based simulation module, a clock-based description and behavioral synthesis information, said behavioral synthesis information including information for describing which of alternative types of storage units are to be simulated; and executing a clock-based simulation in said clock-based simulation module.
14. (New) The method of claim 13, further comprising:  
calculating a power consumption factor based upon both the clock-based description and type of storage unit information.
15. (New) The method of claim 13, wherein said clock-based description is received as an output from a behavioral synthesizing unit, based upon an algorithm description received by said behavioral synthesizing unit.
16. (New) The method of claim 13, wherein said information on storage unit type is received as an output from a behavioral synthesizing unit, based upon an algorithm description received by said behavioral synthesizing unit.
17. (New) The method according to claim 14, wherein the power consumption factor comprises at least one of a toggle rate and a transition probability.
18. (New) The method according to claim 13, further comprising:  
assuming a correspondence between RT variable names and gates from the behavioral synthesis information;  
setting at least one of toggle rates and transition probabilities in gate circuits; and  
calculating toggle rates and transition probabilities of all gate circuits.
19. (New) The method according to claim 18, wherein, if a gated clock is provided, the toggle rate and/or transition probability of a clock are made the same as the write probability with respect to a storage element.